**The University of Jordan**
**College of Engineering & Technology**
**Department of Computer Engineering**
Spring Term – A.Y. 2020-2021

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| **Course:** | Advanced Digital Design – 0917434 (3 Cr. – Core Course) |
| **Catalog Data:** | Revision of combinational and sequential circuits. Optimizations and tradeoffs of combinational and sequential designs. Handling glitches and hazards in combinational logic. Describing and testing combinational and sequential logic using Verilog. Synthesis of combinational and sequential logic in addition to post-synthesis tasks. RTL design. Storage devices. Phyiscal implementation on ICs and programmable logic. Introduction to Asynchronous digital circuits. |
| **Prerequisites by Course:** | 0917335 Computer Architecture and Organization 1 |
| **Prerequisites by Topic:** | Students are assumed to have had sufficient knowledge pertaining digital logic design |
| **Textbook:** | Digital Design with RTL design, VHDL, and Verilog, Frank Vahid, 2nd edition, John Wiley and Sons, 2010. |
| **References:** | • Advanced Digital Design with the VERILOG HDL, Michael D. Ciletti, 2nd edition, Pearson, 2011.<br>• Verilog HDL: A Guide to Digital Design and Synthesis, Samir Palnitkar, 2nd edition, Prentice Hall PTR, 2003. |
| **Course Website:** | MS Teams |
| **Schedule & Duration:** | 15 Weeks, 45 lectures, 50 minutes each (including exams). |
| **Minimum Student Material:** | Text book, class handouts, some instructor keynotes, calculator and access to a personal computer and internet. |
| **Minimum College Facilities:** | Classroom with whiteboard and projection display facilities, library, and computational facilities. |
| **Course Objectives:** | This course aims to famalrize students with the following advances in Digital System Design:<br>1. Designing combinational and sequential digital systems using Verilog HDL.<br>2. Understanding design tradeoffs and optimizing circuits for desired performance.<br>3. Using simulators and design software packages to simulate, test, and synthesize digital systems.<br>4. Implementing digital components using programmable logic and differentiating between various physical implementations. |
| **Course Outcomes and Relation to ABET Program Outcomes:** | Upon successful completion of this course, a student should be able to:<br>1. Design and synthesize combinational logic using Verilog.<br>2. Design and synthesize sequential logic using Verilog.<br>3. Understand design tradeoffs and optimize circuits for desired performance.<br>4. Design simple to medium systems at register-transfer level |

(RTL).
5. Use Modelsim to simulate and test digital systems.
6. Learn how different storage devices work.
7. Understand the differences between various phyiscal implementations of digital systems (Full-Custom, ASIC, Programmable).
8. Use open source tools (e.g. Qflow, Yosys) to synthesize and perform post-synthesis tasks of digital systems.

**Course Topics:**

1. Revision of combinational and sequential circuits.
2. Optimizations and tradeoffs of combinational and sequential designs.
3. Handling glitches and hazards in combinational logic.
4. RTL Design.
5. Designing and testing of digital systems using Verilog HDL.
6. Memory basics and storage devices.
7. Physical implementations of digital systems on ICs.
8. Programmable logic.
9. Introduction to Asynchronous digital circuits.

**Computer Usage:**

Hardware descriptive language programs will be used to design simple to medium scale systems. Modelsim simulator will be used to simulate and test the digital systems. Open source tools (e.g. Qflow, Yosys) will be used to synthesize the digital systems.

**Policies:**

- Attendance is required. Class attendance will be taken every class and the university's polices will be enforced in this regard.
- All submitted work must be yours
- Cheating will not be tolerated
- Check department announcements at: http://www.facebook.com/pages/Computer-Engineering-Department/369639656466107

**Assessments:**

Assignments, Quizzes and Exams.

**Grading policy:**

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| Assignments & Quizzes | 20% |
| Midterm Exam | 30% |
| Final Exam | 50% |

**Instructors:**

Dr. Waleed Dweik, w.dweik@ju.edu.jo
Office Hours: Tuesday: 12:30 – 1:30 PM
Monday, Wednesday: 1:00 – 2:00 PM

**Class Time and Location:**

Sunday, Tuesday, Thursday: 10:30 – 11:30 AM

**Program Outcomes (PO)**

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| **1** | an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics |
| 2 | an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors |
| **3** | an ability to communicate effectively with a range of audiences |
| **4** | an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts |
| **5** | an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives |
| **6** | an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions |
| **7** | an ability to acquire and apply new knowledge as needed, using appropriate learning strategies. |

**Last Updated:** FEBRUARY 21ST, 2021