The University of Jordan

Faculty of Engineering and Technology

Computer Engineering Department

Fall Semester 2016

Course	Computer Design Lab – 0907439 (1 Cr. – Core Lab)
Catalog Description	Using CAD tools, the student designs and simulates the main parts of a computer: the ALU, registers, control unit, cache memory, system bus, memory, and I/O devices. Integration and simulation of computer design.
Prerequisites by Course	Computer Design (0907432 or co-requisite)
Prerequisites by Topic	Students are assumed to have had sufficient knowledge pertaining to digital logic design, MIPS instruction set architecture, computer arithmetic, processor datapath and control design, and single-cycle and pipelined implementations of processors.
Textbook	Patterson and Hennessy. Computer Organization & Design: The Hardware/Software Interface, 5th ed., Morgan Kaufmann, 2014.
References	1. Hennessy and Patterson, Computer Architecture: A Quantitative Approach, 5th ed., Morgan Kaufmann, 2011. 2. S. Palnitkar, Verilog HDL, 2nd Ed., Prentice Hall, 2003.
Lab Website	https://www.facebook.com/groups/1806437689628910/ Includes lab resources such as: 1. Verilog Manual: D. Hyde, Handbook on Verilog HDL 2. Experiments descriptions 3. The basic Verilog library used (lib439.v)
Schedule & Duration	15 Weeks, 12 labs, 3 hr. each (including exams)
Student Material	Text book, class handouts, some instructor keynotes, and access to a personal computer and the internet.
College Facilities	Lab with whiteboard and projection display facilities, personal computers, and server.
Lab Objectives	The objectives of this course are: 1. Give the students skills in complex logic design, particularly skills needed to design a processor's datapath and control and simple memory components. 2. Introduce the students to hardware description languages and CAD tools used in complex logic design. 3. Give the students skills in testing the correctness and performance of logic designs using proper CAD tools.
Course Outcomes and Relation to ABET Program Outcomes	Upon successful completion of this lab, a student should be able to: 1. Design simple pipelined processor datapath and control and simple memory modules [a, c]. 2. Design and carry out experiments to validate designs of a processor and to assess its performance [b]. 3. Use CAD tools to develop and test designs of a processor [k].

Lab Schedule

Date (Week Start)	Event
4/9/2016	*Lab Preparations*
18/9/2016	First Meeting: Syllabus Distribution
25/9/2016	**Exp 1**: Introduction to Verilog
2/10/2016	**Exp 2**: ALU Design
9/10/2016	**Exp 3**: Register File
16/10/2016	**Exp 4**: Memory Units and ***Quiz 1***
23/10/2016	**Exp 5**: Control Unit
30/10/2016	***Midterm Exam***
6/11/2016	**Exp 6**: Single-Cycle Implementation
13/11/2016	**Exp 7**: Pipelining Implementation
20/11/2016	**Exp 8**: Resolving Data Hazards and ***Quiz 2***
27/11/2016	**Exp 9**: Resolving Control Hazards
TBA	*Final Exam*

Policies

- Attendance is required. Lab attendance will be taken every lab and the university's polices will be enforced in this regard.
- Preparation for each experiment is required before the lab time.
- All submitted work must be yours
- Cheating will not be tolerated
- However, it is allowed to discuss experiments with other students in the class or getting verbal advice/help from students who have already taken the course. But any sharing of code is not allowed.
- Check department announcements at: http://www.facebook.com/pages/Computer-Engineering-Department/369639656466107 for general department announcements.

Assessments

Quizzes, exams, reports, and in-lab assessment

Grading policy

Pre-Lab Preparations	5%
Two Quizzes	15%
Midterm Exam	30%
In-lab Performance and Submitted Code	10%
Final Exam	40%

Instructors

Dr. Fahed Jubair, f.jubair@ju.edu.jo

Engineers

Eng. Amal Quzmar, a.quzmar@ju.edu.jo

Class Time and Location

Section 1: Sun 1:00-4:00pm, Computer Design Lab

Section 2: Mon 12:30-3:30pm, Computer Design Lab

Section 3: Tue 1:00-4:00pm, Computer Design Lab

Last Updated: Sep 16th, 2016

Program Outcomes (PO)

a	An ability to apply knowledge of mathematics, science, and engineering
b	An ability to design and conduct experiment as well as to analyze and interpret data.
c	An ability to design a system, component, or process to meet desired needs , within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
d	An ability to function on multidisciplinary teams
e	An ability to identify, formulate, and solve engineering problems
f	An understanding of professional and ethical responsibility.
g	An ability to communicate effectively
h	The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context
i	A recognition of the need for, and an ability to engage in life-long learning
j	Knowledge of contemporary issues
k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice