Curriculum Vitae

Name WaleedDweik

Academic Rank Assistant Professor

Address Computer Engineering Department, Office: 412

Faculty of Engineering and Technology

The University of Jordan

Amman 11942, Jordan

E-mail: w.dweik@ju.edu.jo

Education

Ph.D.in Computer Engineering **01/2009 to 12/2014**
University of Southern California **Los Angeles, CA**

- GPA: 3.96
- Thesis Title: Low Cost Fault Handling Mechanisms For Multicore And Many-Core Systems
- Supervisor: Prof. MuraliAnnavaram

Master of Science inComputer Engineering **01/2007 to 12/2008**
University of Southern California **Los Angeles, CA**

- GPA: 3.91

BS in Computer Engineering **10/2001 to 10/2005**
University of Jordan Amman, Jordan

- GPA: 3.82 (Graduated ranking 3rd out of 93 students in the class of 2005)

Professional activities in the last five years

Assistant Professor **01/2015 to Present**
University of Jordan **Amman, Jordan**

- Instructing computer organization, digital logic, and embedded systems courses and labs.

Intern **01/2014 to 08/2014**
Intel Corporation **Hillsboro, OR**

- Worked on the performance evaluation of the second-generation of Xeon Phi processer known as Knights Landing.

Research Assistant **08/2008 to 12/2014**
University of Southern California **Los Angeles, CA**

- Developed a simulation infrastructure to quantify the amount of available opportunistic testing proposed in our paper: Continuous Reliability Monitoring Using Adaptive Critical Path Testing.
- Developed a simulation infrastructure which models various types of intermittent faults and relies on accelerated fault injections to evaluate our proposed Reliability Aware Exceptions(RAEs) approach.
- Performed an FPGA-based microprocessor block utilization analysis to motivate our work: Signature-based Adaptive Periodic Testing.

Lecturer **08/2013 to 12/2013**
University of Southern California **Los Angeles, CA**

- Instructed the EE457 class: "Computer Systems Organizations". The class contents include: register transfer level machine organization, performance evaluation, arithmetic, pipelined processors, exceptions, out-of-order and speculative execution, cache, virtual memory, multi-core multi-threaded processors, cache coherence.

Teaching Assistant **08/2008 to 05/2012**
University of Southern California **Los Angeles, CA**

- Conducted discussion sessions and labs for Introduction to Digital Circuits, Computer Systems Organization, Computer Systems Architecture, and Digital System Design classes.

Selected Published Research in the last five years

1. B. Zandian, **W. Dweik**, S. Kang, T. Punihaole, and M. Annavaram. Continuous Reliability Monitoring Using Adaptive Critical Path Testing. *Dependable Systems and Networks (DSN), pages 151-160, 2010*.
2. **W. Dweik**, M. Annavaram, and M. Dubois. Reliability Aware Exceptions. USC EE-Computer Engineering Technical Report, CENG 2011-2.
3. **W. Dweik** and M. Annavaram. Signature-based Online Periodic Fault Tolerance for Microprocessors (Fast Abstract). *Dependable Systems and Networks (DSN), 2012*.
4. **W. Dweik**, M. Annavaram, and M. Dubois. Reliability Aware Exceptions: Tolerating Intermittent Faults in Microprocessor Array Structures. *Design, Automation and Test in Europe (DATE), 2014*.
5. **W. Dweik**, M. AbdelMajeed, and M. Annavaram. Tolerating Hard Faults in GPGPUs. *Dependable GPU Computing workshop at Design, Automation and Test in Europe (DATE), 2014*.
6. **W. Dweik** and M. Annavaram. SignTest: Signature-based Adaptive Periodic Testing. *The 39th Annual GOMACTech Conference, 2014*.
7. **W. Dweik**, M. AbdelMajeed, and M. Annavaram. Warped-Shield: Tolerating Hard Faults in GPGPUs. *Dependable Systems and Networks (DSN), pages 431-442, 2014*.
8. M. AbdelMajeed, **W. Dweik**, H. Jeon, and M. Annavaram. Warped-RE: Low-Cost Error Detection and Correction in GPUs. *Dependable Systems and Networks (DSN), 2015*.