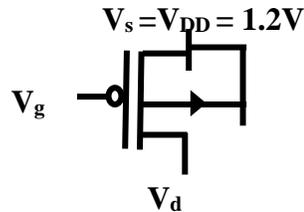


In this lab we will

- Analyze the I-V characteristics of the NMOS and PMOS transistors using LTspice.
- Design a transmission gate
- Test the ability of the NMOS and PMOS transistors to transfer voltage.

PART 1: Transistor Analysis

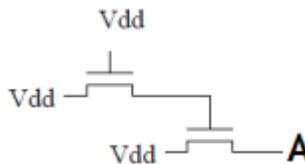
Build the circuit shown in the figure below using **PMOS** transistor and answer the following questions:



- 1- For $W=300n$ and $L=100n$ find the drain current I_d and the mode of operation when the gate voltage is 0.25 V and the drain voltage is 0.2V.
- 2- Draw the I-V characteristics (V_{ds} vs I_{ds}) for the PMOS transistor for the following gate voltage values (0, 0.25, 0.5 and 0.75)
- 3- Draw the relation between the length of the transistor and the current for the values used on Q1.
- 4- Draw the relation between the temperature and the current for the values used on Q1.
- 5- **[Post Lab]** Draw the relation between the body voltage and the current for the values used on Q1.

PART 2: Pass transistors and Transmission Gate

- 1- Using pass transistor design an experiment to measure the V_{th} voltage of an NMOS transistor.
Hint: Connect the gate of the transistor to Vdd and apply a pulse signal at the drain of the transistor.
- 2- Draw the circuit below to find the voltage at Node A.



PART 3: Transmission Gate (Post Lab)

Design a transmission gate using NMOS and PMOS transistors and then design an experiment to test its ability to transfer strong 0 and string 1.

Digital Electronics Lab (CPE 462)

Lab 2

Inverter Design and Analysis

In this lab we will

- Analyze the functionality of the NMOS resistive load inverter .
- Analyze the functionality of the CMOS inverter.
- Design the layout of the CMOS inverter

PART 1: NMOS Resistive Load Inverter (Schematic)

Design an NMOS resistive load inverter with the following parameters: $R_L=7K$, $W=128n$, $L=32n$, Capacitance at output = 40fF and answer the following questions:

- 1- What are the values of V_{OL} and V_{OH} of the inverter?
- 2- Change the value of W and show its impact on the Inverter characteristics.

Parameter	V_{OH}	V_{OL}	$I_C(V_{in}=0)$	$I_C(V_{in}=1)$
$W \uparrow$				

- 3- Calculate the average power of one cycle. Assume the cycle time is 100n with 40% duty cycle

PART 2: CMOS Inverter (Schematic)

Design CMOS inverter with the following parameters: $W_n=64n$, $L_n=32n$, $W_p=128n$, $L_p=32n$ Capacitance at output = 60fF and answer the following questions:

- 1- What are the values of V_{OL} and V_{OH} of the inverter?
- 2- What is the current of the NMOS and PMOS transistors when $V_{in}=0$ and $V_{in}=1$.
- 3- Calculate the average power of one cycle.

PART 3: CMOS Inverter (Layout)

Design CMOS inverter with the following parameters: $W_n=64n$, $L_n=32n$, $W_p=128n$, $L_p=32n$ Capacitance at output = 60fF and answer the following questions:

- 1- What are the values of V_{OL} and V_{OH} of the inverter?
- 2- What is the current of the NMOS and PMOS transistors when $V_{in}=0$ and $V_{in}=1$.
- 3- Calculate the average power of one cycle.
- 4- Compare the rise time and the fall time of the Layout and schematic versions of the inverter.

Note: Please watch this video on how to use Electric to design the layout.

<https://youtu.be/Jqj8VmS38fw>

Instructions on Simulating Layout Using LTspice

Layout simulation using LTspice

1- In our class we will not use the **C5_models.txt** file that is used in the tutorial. Instead we will use the **32nm** technology models. You can find the file **Tech_models.txt** on MS teams under the Files tab. In your spice code use Tech_models.txt instead of C5_models.txt.

2-To setup the simulator to use LTspice follow these steps

1. In Electric Go to **File->Preferences**.
2. In the open window expand the **Tools** directory that appears on the right side of the window
3. click on Spice/CDL
4. In the **Running Spice** section fill the **Run Program** part with the path to the **XVIIx64.exe** file on your PC. It is the file that we execute when we launch LTspice.. You can find it inside **program files\LYC\LTspiceXVII**
5. Fill the **With Args** textbox with the following text (**COPY THE TEXT AS IT IS including the double quotation mark**)

```
"-i ${FILENAME} -r ${FILENAME_NO_EXT}.raw -o ${FILENAME_NO_EXT}.out"
```

To avoid any errors use the following spice code to simulate the 2 input NAND gate

```
vdd VDD 0 DC 1.2 vin A 0 PULSE(0 1.2 0 1n 1n 20n 40n 5)
vin2 B 0 PULSE(0 1.2 0 1n 1n 40n 80n 5)
load OUT 0 50fF
.tran 0 40n .include C:\\Tech_models.txt (Fill the right path to the Tech_models.txt file)
```

Please let me know if you need any help

Digital Electronics Lab (CPE 462)

Lab 3

Combinational Circuit Design

In this lab we will

- Design the schematic for the basic logic gates
- Analyze the performance and power of the schematic of the basic gates
- Design the layout for the basic logic gates
- Analyze the performance and power of the layout of the basic gates
- **Note: In all questions assume that load capacitance is 60fF.**

PART 1A: NAND gate (Schematic)

Design the schematic of the 3-input NAND gate and answer the following questions

- 1- Test all input combinations for the gate
- 2- Size the transistors such that the worst case rise and the fall time are almost the same.
- 3- Measure the average power of the NAND gate 1ns before the transition and 1ns after the transition of the input signal.

PART 1B: NOR gate (Schematic)

Design the schematic of the 3-input NOR gate and answer the following questions

- 1- Test all input combinations for the gate
- 2- Size the transistors such that the worst case rise and the fall time are almost the same.
- 3- Measure the average power of the NOR gate 1ns before the transition and 1ns after the transition of the input signal.

PART 2A: NAND gate (Layout)

Draw the stick diagram of the 2-input NAND gate and then Design the layout of the gate before answering the following questions

- 1- Test all input combinations for the gate
- 2- Size the transistors such that the worst case rise and the fall time are almost the same.
- 3- Measure the average power of the NAND gate 1ns before the transition and 1ns after the transition of the input signal.

PART 2B: NOR gate (Layout)

Draw the stick diagram of the 2-input NOR gate and then Design the layout of the gate before answering the following questions

- 1- Test all input combinations for the gate
- 2- Size the transistors such that the worst case rise and the fall time are almost the same.
- 3- Measure the average power of the NOR gate 1ns before the transition and 1ns after the transition of the input signal.

PART 3: NOR gate using Transmission gates and inverters (schematic)(Post Lab)

Design 2-input NOR gate using transmission gates and inverters only and answer the following questions:

- 1- Test all input combinations for the gate
- 2- Size the transistors such that the worst case rise and the fall time are almost the same.
- 3- Measure the average power of the NOR gate 1ns before the transition and 1ns after the transition of the input signal.

Note: Please watch this video on how to use Electric to design the layout.

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Digital Electronics Lab (CPE 462)

Lab 3

Combinational Circuits Layout

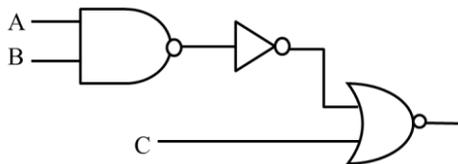
In this lab we will

- Design and Analyze the functionality of the Combinational circuits layout built as complex function and using standard cells.

PART 1: Standard Cell Design (Schematic)

Given the NAND, NOR and Inverter gates layouts build the layout for the following functions.

- 1- Test the functionality of the design using all input combinations
- 2- What is the rise time of the design when the input changes from ABC = 000 to ABC = 101



PART 2: Design the layout for the following expression as a complex function.

- 1- Draw the schematic of the expression
- 2- Draw the stick diagram
- 3- Based on the stick diagram design the layout of the expression.

$$F = \overline{A \cdot B + C}$$

PART 3: NOR gate using Transmission gates and inverters (schematic)(Post Lab)

Design 2-input NOR gate using transmission gates and inverters only and answer the following questions:

- 1- Test all input combinations for the gate
- 2- Size the transistors such that the worst case rise and the fall time are almost the same.
- 3- Measure the average power of the NOR gate 1ns before the transition and 1ns after the transition of the input signal.

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load OUT 0 50fF
.tran 0 40n .include C:\\Tech_models.txt (Fill the right path to the Tech_models.txt file)
```

Please let me know if you need any help

Digital Electronics Lab (CPE 462)

Lab 5

Combinational Circuit Design

In this lab we will

- Design the schematic for the basic logic gates using Pseudo-NMOS, Dynamic and Domino Logic
- Compare the power of the dynamic logic against the CMOS Circuits.
- **Note: In all questions assume that load capacitance is 60fF.**
- **In all experiments measure the power for the**

PART 1A: Pseudo-NMOS Inverter (Schematic)

Design the schematic of the inverter using Pseudo-NMOS transistor

- 1- What is the relation between the width of the PMOS transistor and Logic 0
- 2- What is the power for one cycle?

PART 1B: Dynamic Inverter gate (Schematic)

Design the schematic of the CMOS Inverter and the Dynamic Inverter and answer the following questions:

- 1- Test the functionality of the inverter
- 2- Create a symbol for each inverter
- 3- Measure the FO4 delay of the inverter
- 4- Measure the power of the FO4 inverter (inverter driving 4 similar inverters)

PART 2A: NAND gate (Schematic) (Post Lab)

Design the schematic of the CMOS 2-Input NAND and the Dynamic 2-Input NAND and answer the following questions:

- 1- Test the functionality of the NAND
- 2- Create a symbol for each NAND
- 3- Measure the FO4 delay of the NAND
- 4- Measure the power of the FO4 NAND

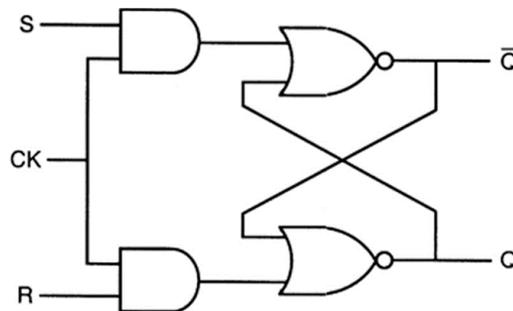
Digital Electronics Lab (CPE 462)

Lab 6

Sequential Circuit Design (Part 1)

In this lab we will

- Design the schematic for the Clocked SR latch and analyze its functionality
- Design the layout for the Clocked SR latch and analyze its functionality
- Design the schematic for the Master-Slave D Flip Flop and analyze its functionality



PART 1: Clocked SR latch (Schematic)

Design the schematic for Clocked SR latch and verify its functionality

- 1- Measure the D-to-Q delay propagation delay of the latch
- 2- Measure the Clk-to-Q delay of the latch

PART 2: Clocked SR latch (Layout) (Post lab)

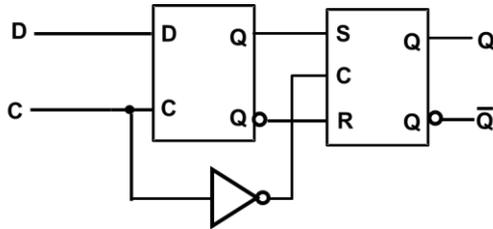
Design the layout for Clocked SR latch and verify its functionality

- 1- Measure the D-to-Q delay propagation delay of the latch
- 2- Measure the Clk-to-Q delay of the latch

Digital Electronics Lab (CPE 462)
Lab 6
Sequential Circuit Design (Flip flops)

In this lab we will

- Design the schematic for the Master-Slave D Flip Flop and analyze its functionality
- Design the schematic for the Master-Slave D Flip Flop and analyze its functionality



PART 1: D-Master-Slave FF (Schematic)

Design the schematic for the D-Master-Slave FF and verify its functionality:

- 1- Measure the D-to-Q delay propagation delay of the FF
- 2- Measure the Clk-to-Q delay of the FF
- 3- Measure the setup time for the FF
- 4- Measure the hold time of the FF

PART 2: D-Master-Slave FF (layout)(Post lab)

Design the layout for the D-Master-Slave FF and verify its functionality:

- 1- Measure the D-to-Q delay propagation delay of the FF
- 2- Measure the Clk-to-Q delay of the FF
- 3- Measure the setup time for the FF
- 4- Measure the hold time of the FF

Digital Electronics Lab (CPE 462)

Lab 8

Memory Cells (6T SRAM Cell)

In this lab we will

- Design the schematic for the SRAM cell and test its functionality.
- Design the layout for the SRAM cell and test its functionality.

For more details about the SRAM operation please watch the video that I uploaded on the class page on MS teams.

Also it is recommended to watch this YouTube to get better idea about the design and testing

https://www.youtube.com/watch?v=IPnQVrzgC-M&ab_channel=SanjayVidhyadharan

PART 1: 6T SRAM Cell (Schematic)

- Design the schematic for 6T SRAM Cell
- Design the schematic for the sense amplifier
- Test the read operation
- Test the write operation

PART 1: 6T SRAM Cell (Layout)

- Design the schematic for 6T SRAM Cell
- Design the schematic for the sense amplifier
- Test the read operation
- Test the write operation