The University of Jordan

School of Engineering

Department of Computer Engineering

Spring Semester 2022/2023

Course	Computer Organization Lab – 0917439 (1 Cr. – Core Lab)
Catalog Description	Using CAD tools, the student designs and simulates the main parts of a computer: the ALU, registers, control unit, cache memory, system bus, memory, and I/O devices. Integration and simulation of computer design.
Prerequisites by Course	Computer Architecture and Organization (1) (0917335)
Prerequisites by Topic	Students are assumed to have had sufficient knowledge pertaining to digital logic design, RISC-V instruction set architecture, computer arithmetic, processor datapath and control design, and single-cycle and pipelined implementations of processors.
Textbook	Patterson and Hennessy. Computer Organization & Design RISC-V Edition: The Hardware/Software Interface, 2nd ed., Morgan Kaufmann, 2020.
References	1. Hennessy and Patterson, Computer Architecture: A Quantitative Approach, 6th ed., Morgan Kaufmann, 2017. 2. J. Hayes. Computer Architecture and Organization, 3rd ed., McGraw-Hill, 1998. 3. M. Mano. Computer System Architecture, 3rd ed., Prentice Hall, 1993.
Lab Website	Microsoft Teams Includes lab resources such as: 1. Verilog Manual: D. Hyde, Handbook on Verilog HDL 2. Experiments descriptions 3. The basic Verilog library used (lib439.v)
Schedule & Duration	15 Weeks, 12 labs, 3 hr. each (including exams)
Student Material	Text book, class handouts, some instructor keynotes, and access to a personal computer and the internet.
College Facilities	Lab with whiteboard and projection display facilities, personal computers, and server.
Lab Objectives	The objectives of this course are: 1. Introduce the students to Verilog, a hardware description language the modeling and simulation of logic circuits. 2. Use Verilog to implement and simulate a single-cycle processor that can execute ALU operations, loads and stores, branches and jumps. 3. Use Verilog to implement and simulate a 5-stage pipelined processor that can execute the same instructions as above.
Course Outcomes and Relation to ABET Program Outcomes	Upon successful completion of this lab, a student should be able to: 1. Write Verilog programs to describe the datapath and control of single-cycle and pipelined processors [1, 2, 6]. 2. Carry out experiments to validate designs of a processor and to assess its performance [6].

Lab Schedule

Description	Week of
Lab Preparations	**26/2/2023**
Exp 0: Syllabus Distribution & Introduction to Verilog **Exp 1**: Introduction to Verilogger Pro	**5/3/2023**
Exp 2: ALU Design	**12/3/2023**
Exp 3: Register File	**19/3/2023**
Exp 4: Memory Units	**26/3/2023**
Exp 5: Control Unit	**2/4/2023**
Exp 6: Single-Cycle Implementation	**9/4/2023**
Break	**16/4/2023**
Midterm Exam	**23/4/2023**
Exp 7: Pipelining Implementation	**30/4/2023**
Exp 8: Resolving Data Hazards	**7/5/2023**
Exp 9: Resolving Control Hazards	**14/5/2023**
Project Submission	**28/5/2023**
Final Exam	**4/6/2023**

Policies

- Attendance is required. Lab attendance will be taken every lab and the university's polices will be enforced in this regard.
- Preparation for each experiment is required before the lab time.
- All submitted work must be yours.
- Cheating will not be tolerated.
- However, it is allowed to discuss experiments with other students in the class or getting verbal advice/help from students who have already taken the course. But any sharing of code is not allowed.
- Check department announcements for general department announcements at: http://www.facebook.com/pages/Computer-Engineering-Department/369639656466107

Assessments

Assignments, exams, reports, and in-lab assessment

Grading policy

Pre-Lab Preparations and In-lab Assessment	15%
Midterm Exam	30%
Assignment and Quiz	15%
Final Exam	40%

Instructors

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Eng. Amal Quzmar, a.quzmar@ju.edu.jo

Class Time and Location

Section 1: Sunday 1:30-4:30 pm, Computer Design Lab

Section 2: Wednesday 10:00-1:00 pm, Computer Design Lab

Section 3: Wednesday 1:00-4:00 pm, Computer Design Lab

Last Updated: Mar 1st, 2023

Program Outcomes (PO)

1	an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
2	an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
3	an ability to communicate effectively with a range of audiences
4	an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts
5	an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
6	an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions
7	an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.