The University of Jordan
School of Engineering
Computer Engineering Department

Academic Year:	2025 / 2026
Semester:	Fall
Course:	0917439 Computer Organization Lab 1 Credit / Dept. Obligatory
Catalog Description:	Using CAD tools, the student designs and simulates the main parts of a computer: the ALU, registers, control unit, cache memory, system bus, memory, and I/O devices. Integration and simulation of computer design..
Prerequisite(s):	Digital Logic Lab 0917432 Computer Architecture and Organization (1) 0917335
Co-requisite(s):	Computer Architecture and Organization (1) 0917335
Background:	Students are assumed to have sufficient knowledge pertaining to digital logic design, RISC-V instruction set architecture, computer arithmetic, processor datapath and control design, and single-cycle and pipelined implementations of processors..
Textbooks:	• Patterson and Hennessy. Computer Organization & Design RISC-V Edition: The Hardware/Software Interface, 2nd ed., Morgan Kaufmann, 2020. .
References:	• Hennessy and Patterson, Computer Architecture: A Quantitative Approach, 6th ed., Morgan Kaufmann, 2017. • J. Hayes. Computer Architecture and Organization, 3rd ed., McGraw-Hill, 1998. • M. Mano. Computer System Architecture, 3rd ed., Prentice Hall, 1993.
Course Website:	Microsoft Teams Includes lab resources such as: 1- Verilog Manual: D. Hyde, Handbook on Verilog HDL 2- Experiments descriptions 3- The basic Verilog library used (lib439.v)
Schedule & Duration:	16 weeks, 12 sessions, 180 minutes each, including exams.
Student Material:	Textbook, lab handouts, some instructor keynotes, calculator and access to a personal computer and internet.
Facilities:	Lab with whiteboard and projection display facilities, personal computers, and server.
Course Objectives:	• Introduce the students to Verilog, a hardware description language the modeling and simulation of logic circuits. • Use Verilog to implement and simulate a single-cycle processor that can execute ALU operations, loads and stores, branches and jumps. • Use Verilog to implement and simulate a 5-stage pipelined processor that can execute the same instructions as above.

Course Outcomes and Relation to ABET Program Outcomes:

Upon successful completion of this course, a student should be able to:

- Write Verilog programs to describe the datapath and control of single-cycle and pipelined processors [**SO1, SO2, SO6**].
- Carry out experiments to validate designs of a processor and to assess its performance [**SO6**].

Lab Schedule:

Week of	Date	Activity/Experiment
1	05/10/25	Lab Preparations
2	12/10/25	**Exp 0**: Syllabus Distribution & Introduction to Verilog **Exp 1**: Introduction to Verilogger Pro
3	19/10/25	**Exp 2**: ALU Design
4	26/10/25	**Exp 3**: Register File
5	02/11/25	**Exp 4**: Memory Units + **Quiz**
6	09/11/25	**Exp 5**: Control Unit
7	16/11/25	**Exp 6**: Single-Cycle Implementation
8	23/11/25	**Break or Midterm Exam**
9	30/11/25	**Break or Midterm Exam**
10	07/12/25	**Exp 7**: Pipelining Implementation
11	14/12/25	**Exp 8**: Resolving Data Hazards
12	21/12/25	**Exp 9**: Resolving Control Hazards
13	28/12/25	Project
14	04/01/26	**Project Submission**
15	11/01/26	**Final Exam**

Computer Usage:

In-lab computers to write Vreilog programs to describe the datapath and control of single-cycle and pipelined processors.

Policies:

- Attendance is required. Lab attendance will be taken every lab and the university's polices will be enforced in this regard.
- Preparation for each experiment is required before the lab time.
- All submitted work must be yours.
- Cheating will not be tolerated.
- However, it is allowed to discuss experiments with other students in the class or getting verbal advice/help from students who have already taken the course. But any sharing of code is not allowed.
- Check department announcements for general department announcements at: http://www.facebook.com/pages/Computer-Engineering-Department/369639656466107

Assessment Tools & Grading:

☒ Pre-Lab Preparations and In-lab Assessment	15%
☒ Midterm Exam	30%
☒ Project and Quiz	15%
☒ Final Exam	40%

Instructor(s):

- **Eng. Amal Quzmar**, a.quzmar@ju.edu.jo

Section(s):

- Section 2: Tuesday 1:30-4:30 pm, Computer Design Lab
- Section 3: Wednesday 1:00-4:00 pm, Computer Design Lab

Student Outcomes (SO)

SO1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.

SO2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.

SO3. An ability to communicate effectively with a range of audiences.

SO4. An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts

SO5. An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.

SO6. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.

SO7. An ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

Last modified: October 1, 2025