Course: Field-Programmable Gate Array Architectures FPGA–0908433 (3 Cr. – Elective Course)

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Course Website: https://elearning.ju.edu.jo

Catalog Data: HDL (hardware description language) and FPGA (field-programmable gate array) devices allow designers to quickly develop and simulate a sophisticated digital circuit, realize it on a prototyping device, and verify operation of the physical implementation. As these technologies mature, they have become mainstream practice. We can now use a PC and an inexpensive FPGA prototyping board to construct a complex and sophisticated digital system. This course uses a “learning by doing” approach and illustrates the FPGA and HDL development and design process by a series of examples. A wide range of examples is included, from a simple gate-level circuit to an embedded system with an 8-bit soft-core microcontroller and customized I/O peripherals.

Prerequisites by Course:  
Digital Logic - 0907231

Prerequisites By Topic:  
Students are assumed to have sufficient knowledge pertaining to the following:  
1. Digital Logic fundamentals  
2. Microprocessor and Microcontrollers

Textbook:  

References:  

Schedule & Duration:  
16 Weeks, 32 lectures (50 minutes each) plus 12 Lab (150 minutes each) and exams.

Minimum Student Material:  
Textbook, class handouts, scientific calculator, and an access to a personal computer.

Minimum College Facilities:  
Classroom with whiteboard and projection display facilities, library, and computational facilities.
Course Objectives:
1. Recognize the concept of digital system design
2. Identify the benefits and requirements FPGA
3. Provide the student with the knowledge in the Field Programmable Gate Arrays (FPGA), and VERILOG programming language

Course Learning Outcomes and Relation to ABET Student Outcomes:
Upon successful completion of this course, a student should:

- Know how to build Digital System (c, e)
- Know the different types of FPGAs (a)
- Improve presentation skills, report writing skills, teamwork skills and problem solving skills due to the work on the project in this course (g, d, i)
- Understand the principle of operation of FPGA (a, e)
- Know how to use verilog in building FPGA applications (k)

Mapping to Student Outcomes

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<th>ABET SO</th>
<th>a</th>
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Course Topics:

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<th>Topic Description</th>
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<td>1. Introduction to ASICs and FPGAs</td>
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<td>2. Fundamentals in digital IC design</td>
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<td>3. FPGA &amp; CPLD Architectures</td>
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<td>4. FPGA Programming Technologies</td>
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<td>5. Introduction to Verilog HDL and FPGA Design flow with using Verilog HDL</td>
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<td>6. FPGA Programmable Interconnect and I/O Ports</td>
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<td>7. Timing Issues in FPGA Synchronous Circuits</td>
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<td>8. FPGA Arithmetic Circuits</td>
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<td>9. FPGAs in DSP Applications</td>
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Ground Rules: Attendance is required and strictly enforced. To that end, attendance will be taken every lecture; Absence of more than 7 hours will result in the expulsion of the student from the course.

Assessments: Exams, Quizzes and Projects.

Grading
Quizzes 10%

Structure:
Midterm Exam 30%
Project 20%
Final Exam 40%

Total 100%

Last updated: Feb 2017