The University of Jordan
School of Engineering
Department of Computer Engineering
Spring Term – A.Y. 2022-2023

Course:	Digital Logic Lab – 0907234 (1 Cr. – Core Course)
Catalog Data:	Experiments on basic TTL and CMOS logic gates, including simulations to explore functionality and timing parameters. Experiments using both simulation and practical hardware implementation on FPGAs, using Verilog for combinational and sequential circuits including multiplexers, demultiplexers, decoders, encoders, shift registers, counters, latches and memory. Experiments in logic design using state machines.
Prerequisites by Course:	0907231 Digital Logic
Prerequisites by Topic:	Students are assumed to have had sufficient knowledge pertaining Boolean algebra, design and analysis of combinational and sequential logic circuits.
Textbook:	Logic and Computer Design Fundamentals, M. Morris Mano and Charles R. Kime, 5th edition, Prentice Hall, 2016.
References:	• Digital Design: Principles and Practices, Fourth Edition. John F. Wakerly. Prentice Hall, Upper Saddle River, NJ, 2006. • Altera DE2 Development and Education Board User Manual. • A Simple Design in VHDL Using Altera Quartus II 8 Web Edition.
Course Website:	MS Teams
Schedule & Duration:	12 Weeks, 12 lab sessions, 180 minutes each (including exams).
Minimum Student Material:	Text book, class handouts, some instructor keynotes, calculator and access to a personal computer and internet.
Minimum College Facilities:	Lab with whiteboard and projection display facilities, library, and computational facilities.
Course Objectives:	The objective of this course is to give hands-on experience on desiging, implementing and testing of various logic circuits using discrete components and Verilog HDL.
Course Outcomes and Relation to ABET Program Outcomes:	Upon successful completion of this course, a student should be able to: 1. Build and realize basic logic functions from discrete integrated circuits using breadboards [1, 6]. 2. Use modern synthesis tools to build and simulate schematic combinational and sequential logic circuits and deploy them on FPGAs [1, 6]. 3. Use Verilog hardware descriptive language to build, simulate and synthesize decoders, encoders, multiplexors, arithmetic circuits, sequential circuits and memory units using FPGAs [1, 6]. 4. Work within a team to formulate, design and simulate a logic circuit based on a formal description [1, 2, 5].

Course Topics and Schedule:

Description	Week of
Lab Syllabus and Introduction	26/2/2023
Exp1. Introduction to Altera and schematic programming	5/3/2023
Exp2. Introduction to Verilog programming	12/3/2023
Exp3. Implementation Using Bread boards and Discrete Gates + **Quiz**	19/3/2023
Exp4. Decoder/Encoder Applications	26/3/2023
Exp5. Multiplexers/Demultiplexers Design and Implementation (Time Division Multiplexing)	2/4/2023
Exp6. Arithmetic Circuits Design and Implementation & **Project Assignment**	9/4/2023
Midterm	16/4/2023
Exp7. Latches and Flip-Flops	30/4/2023
Exp8. Registers and Counters	7/5/2023
Open Lab (Project Preparation)	14/5/2023
Project Discussions	21/5/2023

Computer Usage:

Students will use Quartus II software to design, simulate and synthesize their circuits on the Altera FPGA. The free Web Edition of Quartus II can be downloaded using this link:

https://drive.google.com/file/d/17pmtoLtK77f9Yf7O6M_AlaK4Y5aeNd4X/view?usp=sharing

General Polices:

1. Lab attendance will be taken and the university's polices will be enforced in this regard. Two absents are maximally allowed.
2. No makeups are allowed under any circumstances.
3. Cheating will not be tolerated. All submitted work must be yours.

Grading policy:

In-Lab Reports	15%
Quiz	5%
Midterm Exam	25%
Project	15%
Final Exam	40%

Instructors:

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Program Outcomes (PO)

1	an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
2	an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
3	an ability to communicate effectively with a range of audiences
4	an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global,

	economic, environmental, and societal contexts
5	an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
6	an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions
7	an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.