## The University of Jordan College of Engineering & Technology Department of Computer Engineering Fall Term – A.Y. 2016-2017

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Course:	Digital Logic Lab – 0907234 (1 Cr. – Core Course)		
Catalog Data:	Experiments on basic TTL and CMOS logic gates, including simulations to explore functionality and timing parameters. Experiments using both simulation and practical hardware implementation on CPLDs or FPGAs, using VHDL for combinational and sequential circuits including multiplexers, demultiplexers, decoders, encoders, shift registers, counters, latches and memory. Experiments in logic design using state machines.		
Prerequisites by Course:	0907231 Digital Logic		
Prerequisites by Topic:	Students are assumed to have had sufficient knowledge pertaining Boolean algebra, design and analysis of combinational and sequential logic circuits.		
Textbook:	Logic and Computer Design Fundamentals, M. Morris Mano and Charles R. Kime, 4 <sup>th</sup> edition, 2008. Prentice Hall, 2008.		
References:	<ul> <li>Digital Design: Principles and Practices, Fourth Edition. John F. Wakerly. Prentice Hall, Upper Saddle River, NJ, 2006.</li> <li>Altera DE2 Development and Education Board User Manual.</li> <li>A Simple Design in VHDL Using Altera Quartus II 6.1 Web Edition.</li> </ul>		
Course Website:	http://logic-ju.ucoz.com		
Schedule & Duration:	16 Weeks, 10 Lab sessions, 180 minutes each (including exams).		
Minimum Student Material:	Text book, class handouts, some instructor keynotes, calculator and access to a personal computer and internet.		
Minimum College Facilities:	Lab with whiteboard and projection display facilities, library, and computational facilities.		
Course Objectives:	The objective of this course is to give hands-on experience on desiging, implementing and testing of various logic circuits using discrete components and Verilog HDL.		
Course Outcomes and Relation to ABET Program Outcomes:	<ul> <li>Upon successful completion of this course, a student should be able to:</li> <li>1. Use breadboards to realize basic logic functions from discrete integrated circuits. [a]</li> <li>2. Conduct experiment with logic circuits in SOP and POS forms using discrete TTL logic gates. [a]</li> <li>3. Design, simulate and synthesize logic circuits of various complexity using Verilog HDL and Altera FPGA. [a,b,k]</li> </ul>		

Course Topics and		Descr	iption	Week of	
Schedule:		Lab Prep	arations	4/9	
	Exp1. Basic Log	<b>Exp1</b> . Basic Logic Gates Implementation Using Bread boards and Discrete Gates.			
	Exp2. Introduction usir	<b>Exp2</b> . Introduction to Altera and schematic programming using Quartus II software.			
		NO LAB			
	Exp3. Introduction t	<b>Exp3</b> . Introduction to Verilog programming using Quartus II Software.			
	Exp4. Combinat	16/10			
	Implei				
	<b>Exp5</b> . D	Exp5. Decoder/Encoder Applications			
	<b>Exp6</b> . Multipl Implementati	<b>Exp6</b> . Multiplexers/Demultiplexers Design and Implementation (Time Division Multiplexing)			
		Practical Exam			
	Exp7. Arithmetic	Exp7. Arithmetic Circuits Design and Implementation			
	Exp	Exp8. Latches and Flip-Flops			
	Exp9	Exp9. Registers and Counters			
	<b>Exp10</b> . Me	Exp10. Memory Design + Written Exam			
		Final E	xam	TBA	
Computer Usage:	Students will use Qu their circuits on the A	Students will use Quartus II software to design, simulate and synthesize their circuits on the Altera FPGA.			
General Polices:	<ol> <li>Class attendance will be taken every class and the university's polices will be enforced in this regard. Two absents are maximally allowed.</li> </ol>				
	<ol> <li>Quizzes will reflect your understanding for previous experiments and your preparing for new experiment.</li> <li>No makeups are allowed under any circumstances for either exams or quizzes.</li> <li>All mobile phones must be turned off during the lab.</li> <li>Cheating will not be tolerated. All work must be yours.</li> <li>Compensations are totally not allowed.</li> </ol>				
Assessments:	Lab reports and exa	Lab reports and exams.			
Grading policy:	Pre-Lab Reports	5%			
	In-Lab Reports Practical Exam Written Exam Quiz Final Exam	10% 25% 15% 5% 40%			
Instructors:	Dr. Fahed Jubair Dr. Mohammad Abd Eng. Asma Abedelka Eng. Amal Quzmar Eng. Ola Jaloudy Eng. Alaa Arabiyat Eng. Alaa thaher	el-Majeed arim	f.jubair@ju.edu.jo m.abdel-majeed@ju.edu.jo a.abdelkarim@ju.edu.jo a.quzmar@ju.edu.jo o.jaloudy@ju.edu.jo a.arabiyat@ju.edu.jo al.thaher@ju.edu.jo		

## Program Outcomes (PO)

a	An ability to apply knowledge of mathematics, science, and engineering
b	An ability to design and conduct experiment as well as to analyze and interpret data.
c	An ability to design a system, component, or process to meet desired needs, within realistic constraints such as
	economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
d	An ability to function on multidisciplinary teams
e	An ability to identify, formulate, and solve engineering problems
f	An understanding of professional and ethical responsibility.
g	An ability to communicate effectively
h	The broad education necessary to understand the impact of engineering solutions in a gloabal, economic,
	environmental, and societal context
i	A recognition of the need for, and an ability to engage in life-long learning
j	Knowledge of contemporary issues
k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

Last Updated:

SEP 16, 2016